
# MEARS Technologies

MEARS Technologies
*Quantum Engineered Materials*

K2 ENERGY LIMITED

## Merger with K2 Energy Ltd (KTE.ASX) & Equity Raising

**February 2013**

NOT FOR DISTRIBUTION OR RELEASE IN THE UNITED STATES

# Contents

# Transaction Overview

## Acquisition Transaction

- K2 Energy ('K2') owns 5.3% of MEARS common shares and 13.4% of MEARS fully diluted capital
- Merger agreement for K2 to acquire 100% of outstanding equity securities in the capital of MEARS
- Consideration of approx. 85 million K2 ordinary shares priced at $0.30 each (Merger Shares) [1]
- Consideration valued at approximately $25.5 million
- Final closing date subject to completion of Placement and other closing conditions

## Placement Transaction & ASX Listing

- Placement of 33.3 million K2 ordinary shares at $0.30 to raise up to $10 million (min $7.5 million)
- Pre-money value of approx. $32.8 million; post-money value of approx. $42.8 million
- Completion contemporaneous with completion of acquisition transaction
- ASX listing to be used as a precursor to NASDAQ given market cap & influence of Australian investors in Mears

## Ownership and other changes

| Capital Structure | A$m | Shares (m) | % |
|---|---|---|---|
| K2 Shares outstanding | 7.3 | 24.4 | 17.1 |
| Merger Shares to be issued | 25.5 | 85.0 | 59.6 |
| Placement Shares | 10.0 | 33.3 | 23.3 |
| **Total** | **42.8** | **142.7** | **100.0** |

- K2 10:1 share consolidation
- Company name change to 'MEARS Technologies Limited'
- Board restructure
- Management restructure

*1. Post a 10 for 1 K2 share consolidation*

# Investment Highlights

| | |
|---|---|
| Product to improve Integrated Circuit Chips | ▪ MEARS has developed a unique reengineered silicon film for CMOS transistors that delivers:<br>▪ significantly reduced power consumption<br>▪ enhanced transistor performance<br>▪ valuable improvements in manufacturing efficiencies (op-ex) and delays major cap-ex spend |
| Product Ready for Market Launch | ▪ Prospective customers = major manufacturers in the US$259B semiconductor Integrated Circuit (IC) market:<br>▪ Top 20 generate US$204B or > 78% of IC industry revenue<br>▪ MEARS focused on rolling out transistor solutions in the Digital segment (US$218B) and Analog segment (US$42B)<br>▪ Technology research complete, successfully tested and now commercializing (Customer Product Qualification) |
| Revenue Model | ▪ IP licensing:<br>▪ >110 granted patents (50+ in US alone) and other patents pending<br>▪ Wafer based royalty income (circa 1-3% of CMOS wafer processing cost)<br>▪ CMOS Technology dominant in IC-Production ( approx.95% ) |
| Experience + Track Record | ▪ Industry leading management team:<br>▪ Founder Dr. Robert Mears revolutionised optical fibre industry through quantum engineered solution<br>▪ CEO Erwin Trautmann ex-Texas Instruments responsible for $billions of chip development and sales<br>▪ COO Ron Cope ex-SyChip, National Semi, Hitachi, Texas Instr.; Corporate and Start-up experience<br>▪ TAB Chairman and Director Dr. Rinn Cleavelin ex-COO for International SEMATECH and ex-Texas Instr. |
| Competitive Advantage | ▪ One Film – Many Benefits – a unique proprietary patented technology:<br>▪ No other technology can deliver such a range of multiple benefits |
| Investment Proposition | ▪ US$60 million invested to date over 10+ years 2001-2012:<br>▪ MST technology broadly applicable across most product segments in $318 billion semiconductor industry<br>▪ 5% of global wafer penetration generates close to US$100 million of annual revenue to MEARS<br>▪ Institutional placement priced at an attractive pre-money valuation of $32.8 million |

# Board & Management Team

- Highly credentialed Board & Management team in place with +100yrs collective experience in the semiconductor industry to lead a successful commercialisation programme and supported by globally recognised Technical & Scientific Advisory Board members.

| John Gerber | Erwin Trautmann | Dr. Robert Mears | Ron Cope |
|---|---|---|---|
| **Non-Executive Chairman** | **Executive Director & CEO** | **Executive Director & CTO** | **COO** |
| ■ Currently Managing Partner of Four Points, a specialty investment group that has raised over $1.8b in capital in the last 10yrs across 40 transactions for real estate and venture capital investments. Mr Gerber is also a Director and CEO of two early stage technology companies in the US.<br>■ Founding shareholder & MEARS Director since 2001. | ■ Over 30yrs of semiconductor industry experience through executive positions at several Fortune 500 companies including Texas Instruments ("TI") as a VP with P&L responsibility for major product lines with annual rev of > US$1.6B.Most recently held Senior VP position at KLA-Tencor the leading supplier of Yield Enhancement Solutions .<br>■ Joined MEARS in September 2011. | ■ Dr. Mears founded MEARS Technologies in 2001.<br>■ Recognized pioneer and leading expert in nano-scale material science and engineering. In the late 1980's, Dr. Mears addressed the challenge of expanding the bandwidth of fiber optic cable by inventing the EDFA.<br>■ Existing K2 Energy Director. | ■ Over 30years of chip industry experience. Held senior management, engineering and operations positions at both semiconductor industry start-ups (VLSI, TelCom, InterConnect Tech, SyChip) and major companies (TI, National Semi, Hitachi). Most recently he was VP of Operations and General Manager at SyChip .<br>■ Joined MEARS in September 2011. |

| Dr. Rinn Cleavelin | Rolf Stadheim | Sam Gazal | Ken Gaunt |
|---|---|---|---|
| **Non-Executive Director** | **Non-Executive Director** | **Non-Executive Director** | **Non-Executive Director** |
| ■ 34 years of experience in the semiconductor industry. Held exec positions of COO for International SEMATECH, Technology Manager for TI's Worldwide Manufacturing Science Technology Center, and TI's Manager for Devices and Manufacturing for External R&D.<br>■ Joined MEARS in September 2011. | ■ Founder and Senior Partner of Stadheim & Grear, a leading patent and intellectual property licensing and enforcement practice, engaging primarily on a contingent fee basis with a focus on representing universities.<br>■ MEARS Director since 2008. | ■ Over 35 years experience as a director of public and private successful companies including Gazal Industries Limited, Winthrop Investments Limited, Country Television Services Limited and Sunshine Broadcasting Network Limited.<br>■ Existing K2 Energy Chairman. | ■ Significant commercial success since founding Electronic Banking Solutions Pty Ltd in 1998, before merging with Cash Card Australia Limited in 2003. Ken is a director of Cash Card Australia Limited and is an investor in many successful businesses in Australia and elsewhere.<br>■ Existing K2 Energy Director. |

# Globally Recognized Advisors

- The Mears Board and Management team are supported by globally recognised Technical & Scientific Advisors with strong networks into corporate and academic organizations.

| Lord Alec Broers, | Dr. James Hutchby | Dr. Luigi Colombo | Prof. Tsu-Jae King Liu | Prof. Mike Payne, FRS |
|---|---|---|---|---|
| **Technical Advisory Board** | **Technical Advisory Board** | **Technical Advisory Board** | **Scientific Advisor** | **Scientific Advisor** |
| ▪ Member of the House of Lords and former Chairman of the Science and Technology Committee. President of the Royal Academy of Engineering from 2001 to 2006. Lord Broers is nanotechnology pioneer who worked for IBM in the United States for 20 years serving on IBM's Corporate Technical Committee and as an IBM fellow, an honour accorded to only 175 individuals since 1963 | ▪ Senior Scientist and formerly Director of Device Sciences with the Semiconductor Research Corporation (SRC). Dr. Hutchby founded and formerly chaired the Emerging Research Device (ERD) Working Group for the International Technology Roadmap for Semiconductors (ITRS). | ▪ A TI Fellow in the External Research Development group at Texas Instruments. Currently responsible for the development of new materials such as graphene and their integration in new device flows for beyond CMOS device technology as part of the Nanoelectronics Research Initiative | ▪ University of California at Berkeley, where she is now Professor of Electrical Engineering and Computer Sciences (EECS) and Associate Dean for Research in the College of Engineering. Her research activities are presently in nanoscale semiconductor devices and technology, and thin-film materials and devices for integrated microsystems and large-area electronics. | ▪ Chair of Computational Physics in the University of Cambridge, UK and is head of the Theory of Condensed Matter (TCM) research group at the Cavendish Laboratory. He has worked on first principles total energy calculations since 1985 and is responsible for many of the technical developments that have led to the widespread adoption of the total energy pseudopotential technique |

# MEARS Overview

## Company Overview & Background

- MEARS develops and licenses CMOS semiconductor technologies (MST) and manufacturing solutions for integrated circuits that:
  - significantly reduce power consumption;
  - improve transistor performance;
  - lower gate leakage;
  - reduce variability and increase design margin;
  - delay next node migration → extending fab life → reducing cap-ex for wafer fabrication facilities
- >110 Patents Granted (others pending)
- Background to Mears:
  - Founded 2001 by Dr. Robert Mears
    - Nano-scale material science and engineering pioneer
    - Invention of EDFA from reengineering silica fiber
    - EDFA expanded the bandwidth of optical cable by more than 1000x (mid-1980s)
  - ~US$60 million raised over 10yrs to conduct R&D of MST CMOS
  - Headquarters: Newton, Massachusetts (USA)
  - 10 Employees (2013)

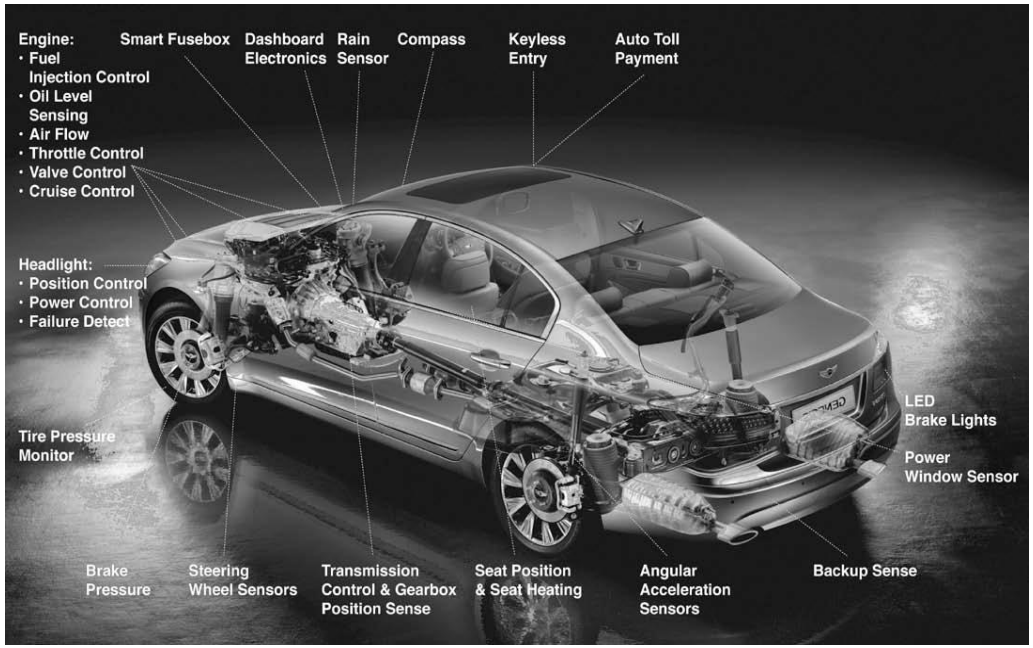
## Focus on Customer

- Focus on the commercialisation phase of MST CMOS – with 95% of the chip industry
- New management team engaged in 2012 with considerable semiconductor industry experience.
- Evaluation of MST already underway with some of the world's leading semiconductor manufacturing companies.
- Targeting first commercial licensing agreement in 2013, with royalty based payments to commence 2014/15

# Semiconductor IC Demand – continuously increasing

**More Systems Functionality – more Electronic Content – more Semiconductor ICs**

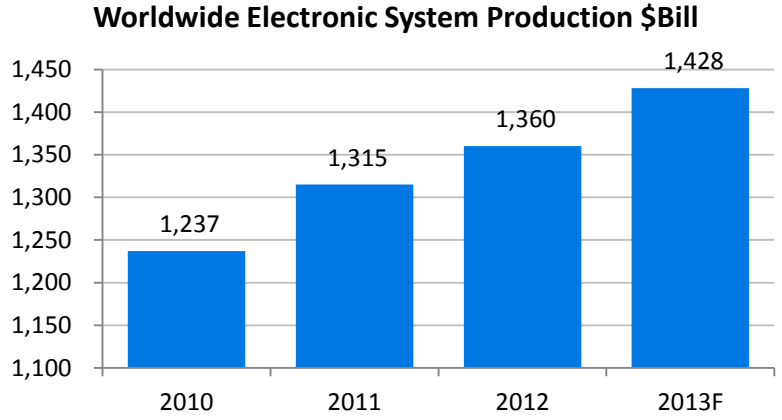
- Increase of electronic content in systems coupled with sophisticated software solutions and applications continue to drive growth in semiconductors.
  - > Increased demand for higher density semiconductor devices.
  - > Un-abated, these increases in performance have a direct impact on chip size, device cost , power consumption and wafer size.
- All are critical issues for battery life and form-factor in **mobile devices** and in **automotive applications** where electronic content is increasing for analog, digital and mixed signal products. (i.e. power train, safety and controls, sensor technology, infotainment, etc.)

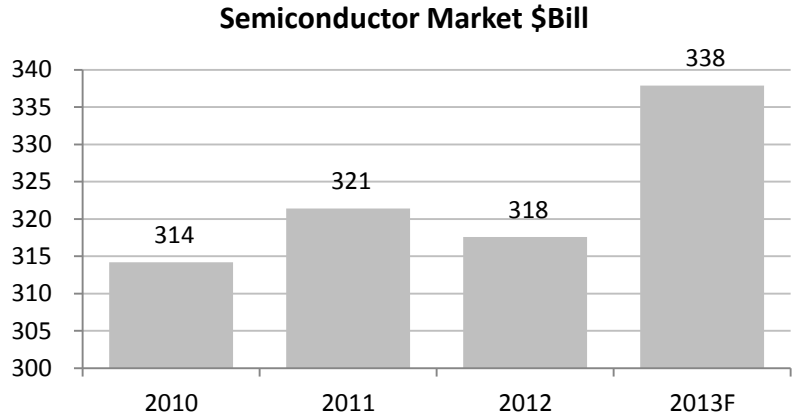

**Transistor Solution:**

- Smaller transistors, less leakage, less power consumption, less variability (more design margin) play a direct role in scalability (more "Moore's Law") and therefore have a direct impact on enabling new IC chip functionality and more functions per wafer area.
- Increase in device functionality comes at a cost and performance enhancements must be affordable.
- **Opportunity for MST™ – better performance, less power, less leakage, more Moore at an affordable cost.**

# 2012 Market Landscape – Electronic Industry Independence




Source: IC Insights 2013



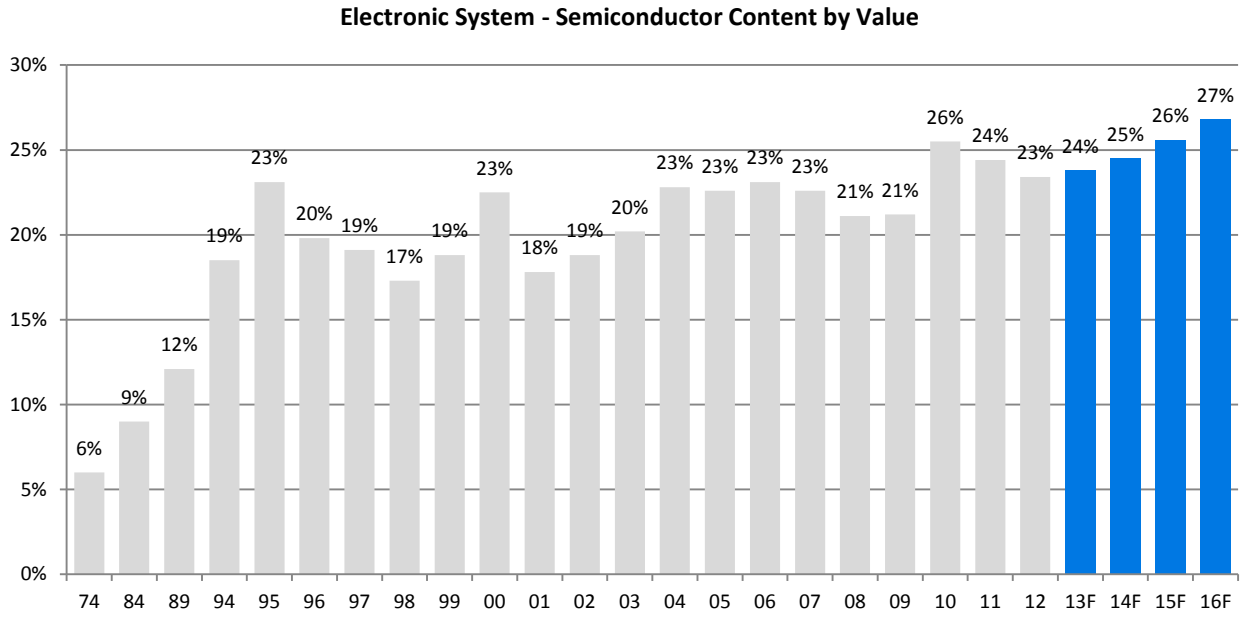

Source: IC Insights 2013

## US$1.36 Trillion Electronics Market

- One of the "Trillion Dollar Markets" along with Energy, Financial, Automotive, Food and Defense.

## US$318 Billion Semiconductor Market

- Integrated Circuit Market at $259B and expected to break $300B in 2014F.
- Increasing Trend of Semiconductor Content in Electronic Systems - 27% in 2016F.



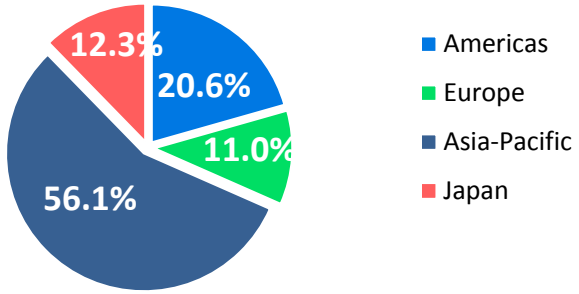

Source: IC Insights 2013

# Global Semiconductor Industry – Markets

## Very Large Industry
2012 | US$

- Global sales $318 billion
- Capital expenditure $59 billion
- R&D expenditure $53 billion
- New 300mm fab $3.8 billion (est. $5.5B by 2016)
- Top 20 chip companies account for 78% of the $259B IC market.
- Asia-Pacific and Japan make up 68% of industry revenue.
- Integrated circuit segmental revenue share: Micro 30%, Memory 24%, Logic 30% and Analog 16%.
- IDMs - integrated device manufacturers that design, produce and market their own chips (e.g. Intel, TI, Micron).
- Fabless – fabless chip companies that design and market, but outsource production (e.g. Broadcom)
- Foundries – companies that manufacture chips to customers' design specifications (e.g. TSMC, GF, UMC).

**Integrated Circuit Revenue by Region**




## Moore's Law & Scaling
2012 | US$

- Making transistors smaller has been a BIG business for 40+ years.
- MOORE'S LAW:
  - every two years the number of transistors on a chip doubles and the unit cost halves.
- SCALING:
  - shrinking the transistor (incl. wafer size increases) has been the principal means for ↑ performance and ↓ cost.
  - 1974 Motorola 6800: 1 MHz | 4,000 transistors | 200 transistors/mm² | ASP $360 (9.0c/transistor).
  - 2011 Intel Core i7: 2.8GHz | 1.1b transistors | 4.2m transistors/mm² | ASP $280 (0.00003c/transistor).

# Global Semiconductor Industry – Technology Challenges



Scaling has Physical Limits and Created Multiple Pain Points

**Limitations in Linear Scaling**

- Performance increases and power consumption efficiencies previously came for "free" with scaling.
- At geometries below 90nm, traditional scaling stops working well and the pain points mount up.

**Industry Pain Points include:**

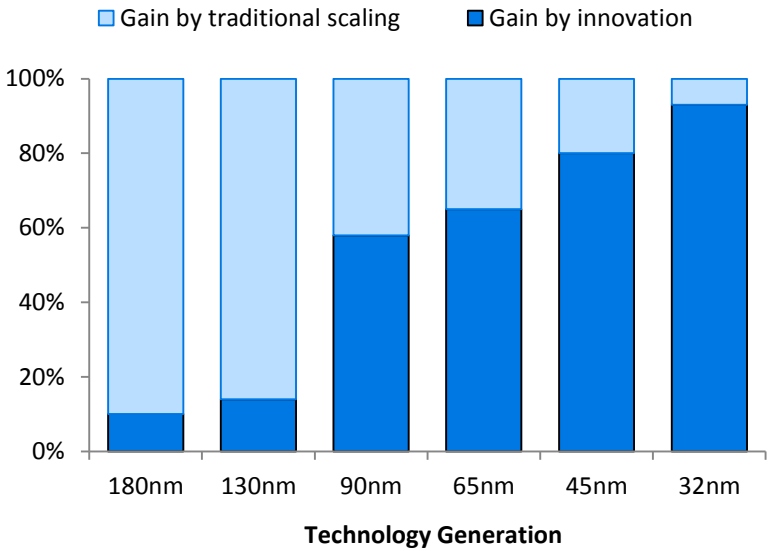
- Reduced Design margins – increased variability
- High power consumption
  - Heat generation, higher leakage
  - Reduced battery life in mobile devices
- Higher cap-ex and operating costs
- Lower manufacturing yields
  - Extensive integration and process complexity
  - New materials, more process steps

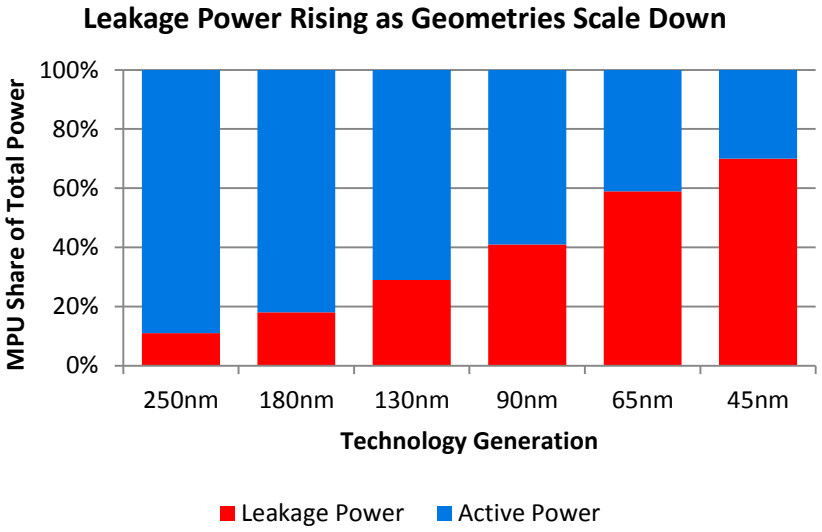
**Structural changes 2006-2011:**

- ↑ industry consolidation: sales revenue share for top 20 chip companies has ↑ from 46% to 65%.
- ↑ outsourcing to foundries: foundries' sales revenue CAGR 7.1% vs. industry CAGR 3.8% .
- More IDMs adopt "Fab Lite Model"

**Innovation**

- **MST™ Opportunity: Increased adoption of new Technologies to extend the CMOS Technology Roadmap.**



# MST™ CMOS – Transistor Solution with Multiple Benefits

## Unique, Novel and Patented Transistor Solution

- **Transistor Solution:** Thin film of engineered silicon approximately 100 atoms thick.
- Replaces the conventional silicon channel in a transistor.
- Delivers multiple scaling benefits through a single technology.
- Widely applicable to most device segments including microprocessor, memory, logic and analog chips.
- Potential to be of substantial value in quest of extending the CMOS Roadmap.
- Trialed and evaluated by several of the world's top ten semiconductor manufacturers.

## One Film: Many Benefits to Address Pain Points

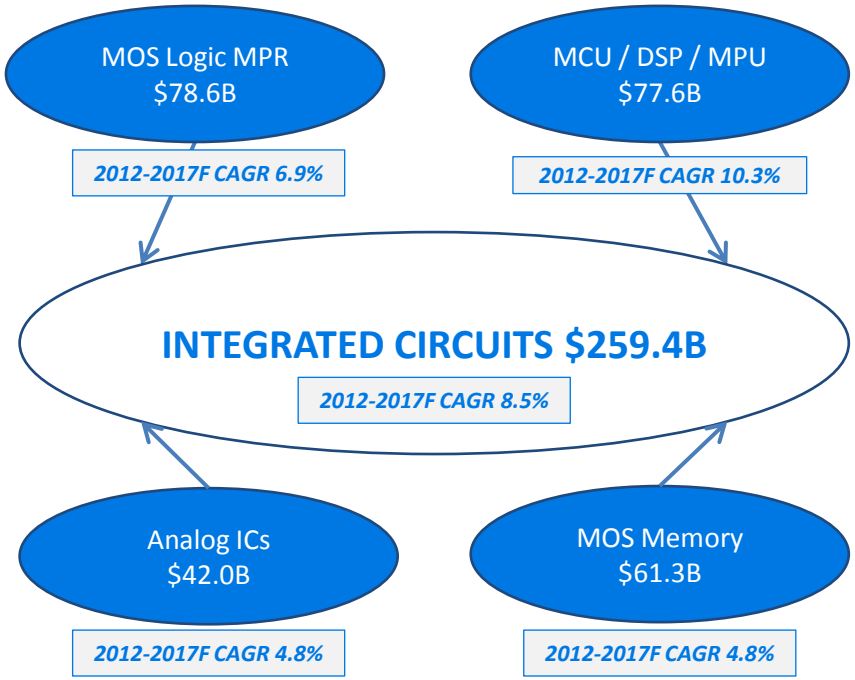
| | | |
|---|---|---|
| **Improved transistor performance** | > | N & P-Channel Transistor (electrons and holes) |
| **Higher mobility (higher gm, higher effective current)** | > | Higher Performance and/or Lower Power |
| **Lower gate leakage** | > | Lower Power and Improved Reliability |
| **Improved matching and variability** | > | Better Design Margin and/or Lower Power |
| **Lower cost – one film** | > | Better Performance/Cost Ratio |

## Significance of MST

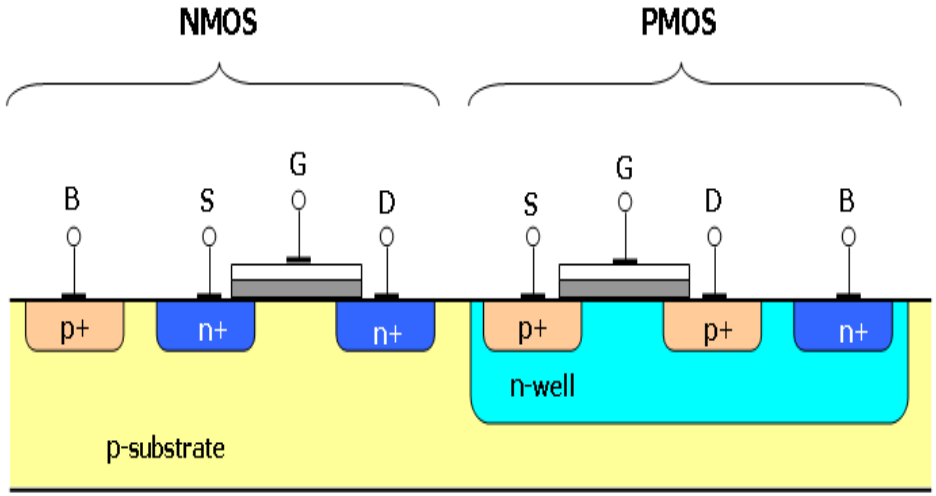
- OEMs are the major Technology Providers to the Industry - including 3rd Party suppliers (e.g.: Tessera, Soitec).
- Industry likes to follow Technology Learning Curve experienced by others before following trend -- MST™ hurdle
- **MST™ Opportunity:**
  - Seek Partnership agreement with established OEM capital equipment maker – customer adoption
  - CMOS Technology is used in over 95% of IC designs -- large market adoption/penetration potential

# The Transistor - Heart of Integrated Circuits

- **The Transistor is the Heart of Integrated Circuit**
- Almost all Semiconductor IC Market Segments are dominated by CMOS Technology.
  - MOS Logic/MPR
  - MPU/MCU/DSP
  - MOS Memory
- Analog Applications of CMOS Technology.
  - Op-Amps, RF Circuits, Transmission Gates,
  - Mixed-Signal Applications (Analog and Digital)




- **CMOS**: **C**omplementary **M**etal **O**xide **S**emiconductor
- **NMOS and PMOS:** N-Channel and P-Channel Transistor
- **CMOS Technology:** Dominant in IC Product Design

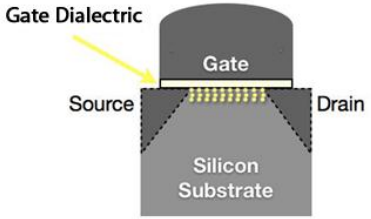



**Definitions:**

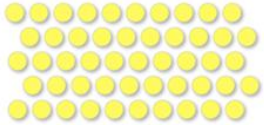
MOS Logic/MPR: Logic Circuit Designs/Multi-Project-Run (Foundry)
MPU/MCU/DSP: Micro Processor Unit/Micro Controller Unit/ Digital Signal Processor
MOS Memory: DRAM, NAND or NOR Flash Memory
Analog IC: RF Circuits, Power Regulators, Mixed Signal Processors, etc.

# MST™ CMOS

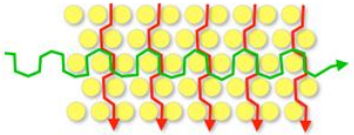
## STANDARD SILICON TRANSISTOR



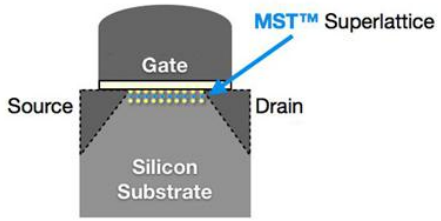

Standard Silicon Atomic Structure



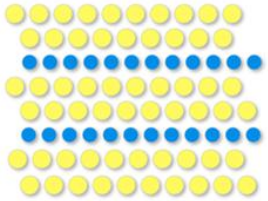
LIMITED Horizontal Current Flow +
EXCESSIVE Vertical Leakage



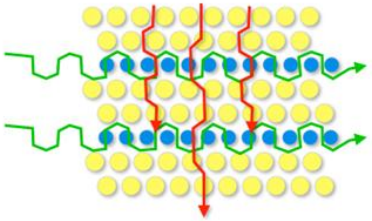
## MST SILICON TRANSISTOR

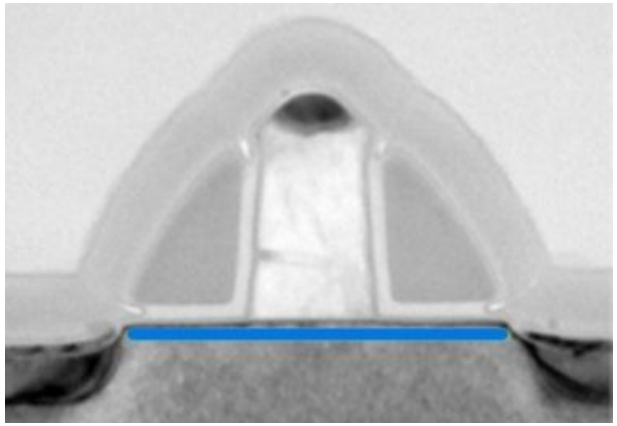


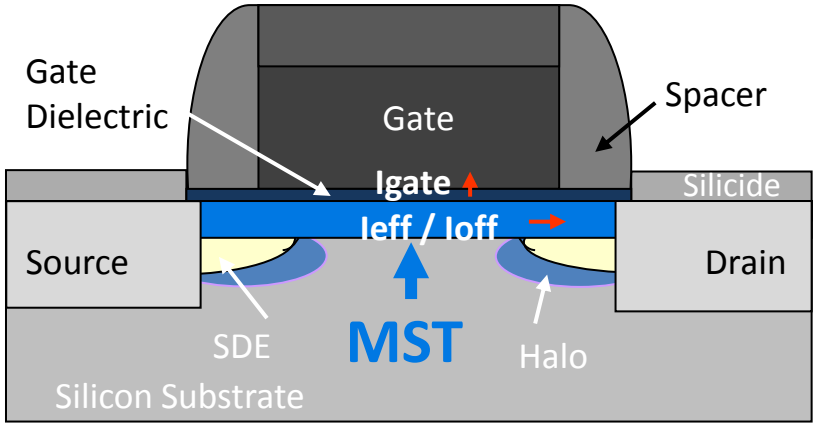

MST™ Silicon Atomic Structure



INCREASED Horizontal Current Flow +
REDUCED Vertical Leakage







# MST™ CMOS -- IP Licensing Business Model

Defensible Value Proposition

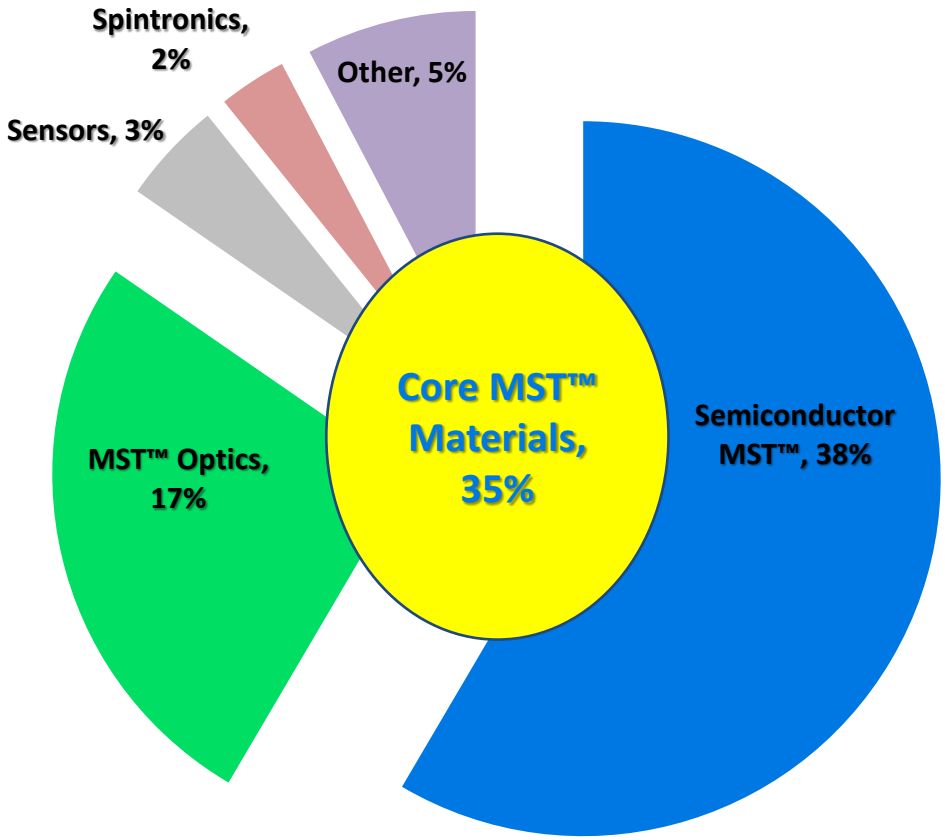
**Business Model:**

- Licensing*
- Patent Development
- Innovation

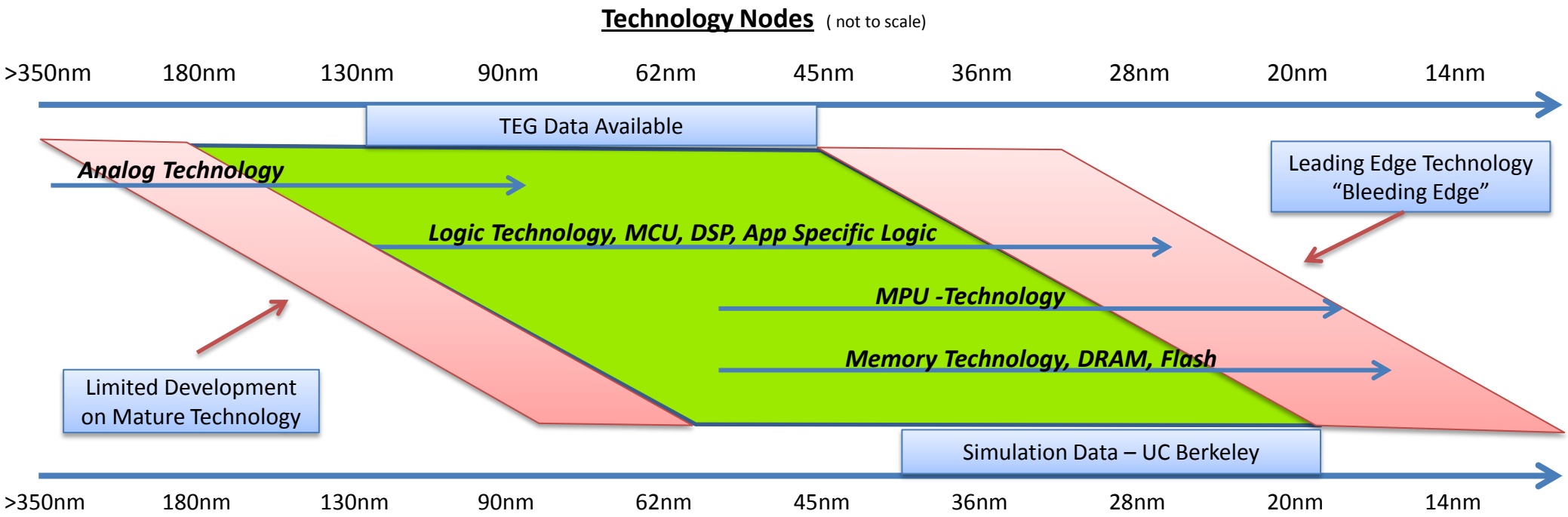
(*) Patents, Trade Secrets, Know How

**Patent Portfolio**

- Patents filed first in the United States
- Core MST™ patents cover both physical structure and process to manufacture
  - > 110 granted patents
  - > 50 granted foreign patents
  - Other patents pending



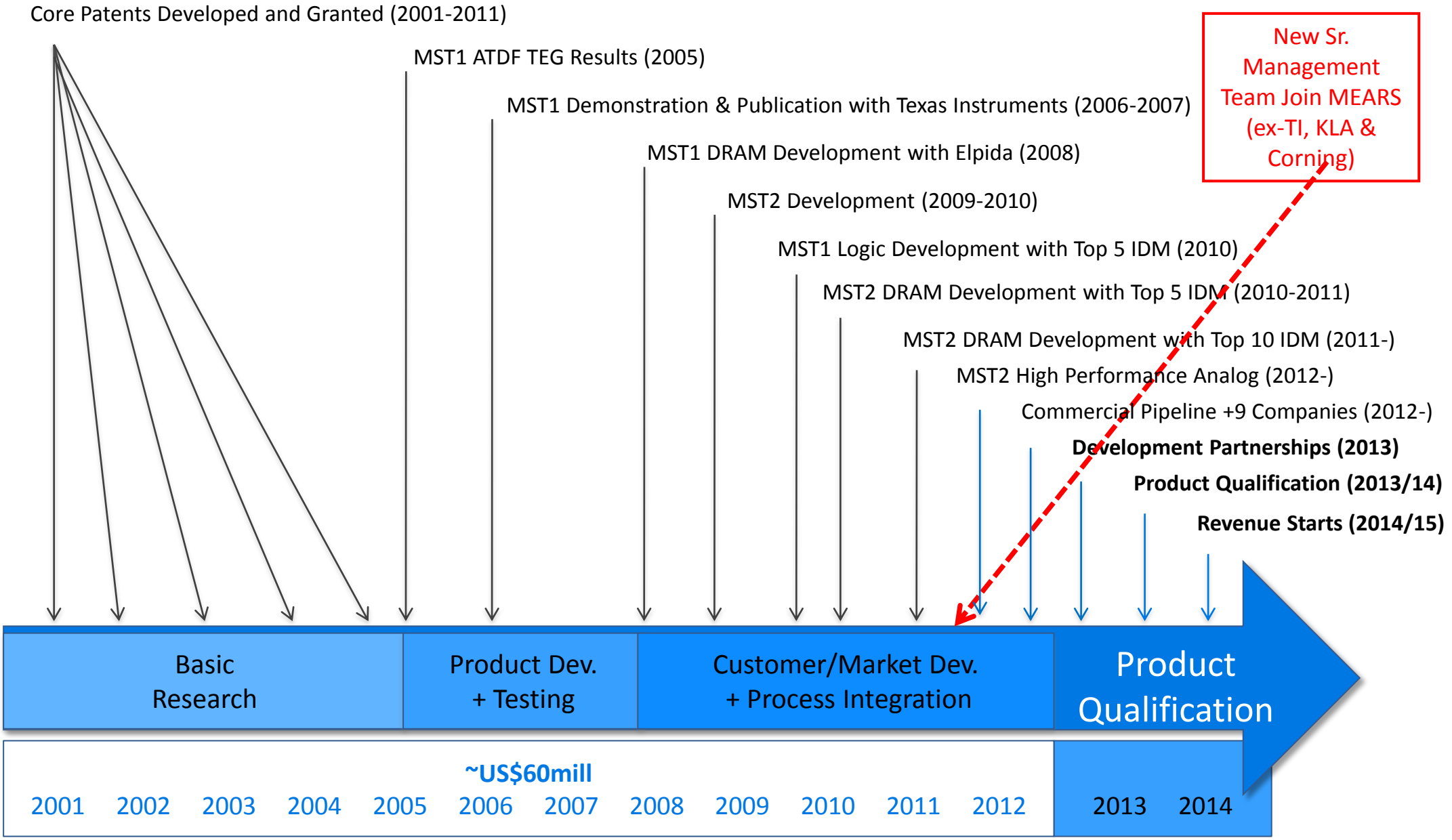
# MST™ CMOS – Technology Opportunity




**Market Opportunity:**

- CMOS MST™ is applicable for a wide spectrum of CMOS Technology from 28nm to >130nm Technology nodes
- Confirmation through customer TEG (test element group) validation, SEMATECH ADTF data and simulation work at UC Berkeley, CA
- Latest work published at IEDM in San Francisco confirmed MST™ application capability all the way to leading edge 20nm Technology node
- Mears focuses on the Logic Market Segment; the business plan is based on conservative market penetration numbers
- In 2012 Mears took advantage of opportunities with customers in the Memory and Analog segment – evaluations are ongoing

# Breakthrough Products – Ready for Commercialisation



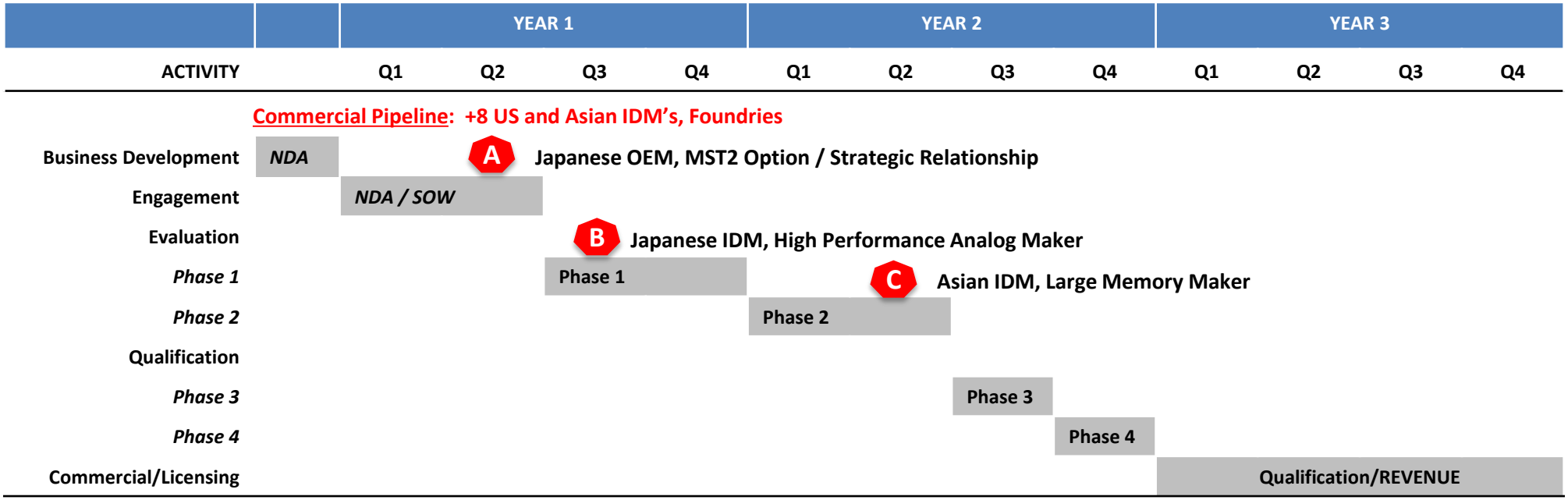
# Significant Market Opportunity

- Very large potential customer base with the top 20 representing 78.6% market share of US$259.4B IC market.
- MEARS commercialisation program commenced mid-2012 – targeting maiden commercial deal 2013.
- Currently engaged with chip companies which in aggregate hold 10-15% market share – including OEM makers supplying capital equipment to the manufacturing fabs
- Focus on the mainstream digital and analog markets representing ~72% of wafer volume (i.e. NOT competing with Intel/Samsung at the bleeding edge)
- Engagements extend across the digital and analog IDMs, Foundries and OEMs.
- Customer markets include: Korea, Taiwan, Japan, US & Europe.
- Marketing strategy includes partnerships with OEM tool manufacturers & sponsorship of university research programs.
- Revenue model to be on a per wafer basis.
  - Commercial deals can equate to 1-3 % royalty of wafer processing cost.
  - Deals will differ by segment and market participant.

| Rank | Company | 2012 | | | |
|---|---|---|---|---|---|
| | | Type | Country | IC Revenue US$Mill | Market Share % |
| 1 | Intel Corporation | IDM | USA | 49,114 | 18.9% |
| 2 | Samsung Electronics | IDM | South Korea | 29,715 | 11.5% |
| 3 | Taiwan Semi Manuf Corp | Foundry | Taiwan | 17,167 | 6.6% |
| 4 | Qualcomm | Fabless | USA | 12,807 | 4.9% |
| 5 | Texas Instruments | IDM | USA | 11,413 | 4.4% |
| 6 | Toshiba Semiconductor | IDM | Japan | 8,905 | 3.4% |
| 7 | SK/Hynix | IDM | South Korea | 8,803 | 3.4% |
| 8 | Renesas Electronics | IDM | Japan/ Sth K | 7,910 | 3.0% |
| 9 | Broadcom | Fabless | USA | 7,815 | 3.0% |
| 10 | Micron Technology | IDM | USA | 7,490 | 2.9% |
| 11 | STMicroelectronics | IDM | South Korea | 6,175 | 2.4% |
| 12 | Advanced Micro Devices | Fabless | USA | 5,422 | 2.1% |
| 13 | Sony | IDM | Japan | 4,905 | 1.9% |
| 14 | Global Foundries | Foundry | USA | 4,560 | 1.8% |
| 15 | NVIDIA | Fabless | USA | 4,224 | 1.6% |
| 16 | Fujitsu Microelectronics | IDM | Japan | 4,037 | 1.6% |
| 17 | UMC | Foundry | Taiwan | 3,730 | 1.4% |
| 18 | MediaTek | Fabless | Taiwan | 3,366 | 1.3% |
| 19 | Freescale Semiconductor | IDM | USA | 3,230 | 1.2% |
| 20 | Marvell | Fabless | USA | 3,121 | 1.2% |
| | **Top 20 Total** | | | **203,909** | **78.6%** |

Source: IC Insights 2013

# Typical Commercialisation Cycle




- **Customer Engagement:** introductory meeting(s), NDA, follow-up detailed technical meeting, Evaluation Agreement; Statement of Work.
- **Phase 1:** First pass customer wafer run with each customer to learn how their process interacts with MST.
  - Future modelling and simulation work will help reduce errors in the first processing run.
- **Phase 2:** Process adjustments based on Phase 1 learning experience.
- **Phase 3:** Confirm integration of MST into customer process , validate electrical performance and add data into design data base.
  - Process conditions may still require final adjustments based on Phase 2 results.
  - IC chips from this phase can potentially be used for pre-qualification work like reliability testing, wafer probe, assembly/test, etc.
- **Phase 4:** Likely to be a set of split lots to populate full qualification. Typically, results from 3 – 5 separately processed lots are required for full qualification and product release. In some cases this may require customer qualification and release as well.
- Process cycle times for Phase 1 & 2 take typically longer; MST™ processing work is currently outsourced to 3rd party (OEM or Service Lab) ; the MST™ film in Phase 3&4 is processed on-site at customer facility.
- **Commercial deals will differ by market segment, technology and wafer type.**

MEARS Technologies
Quantum Engineered Materials

K2 ENERGY LIMITED

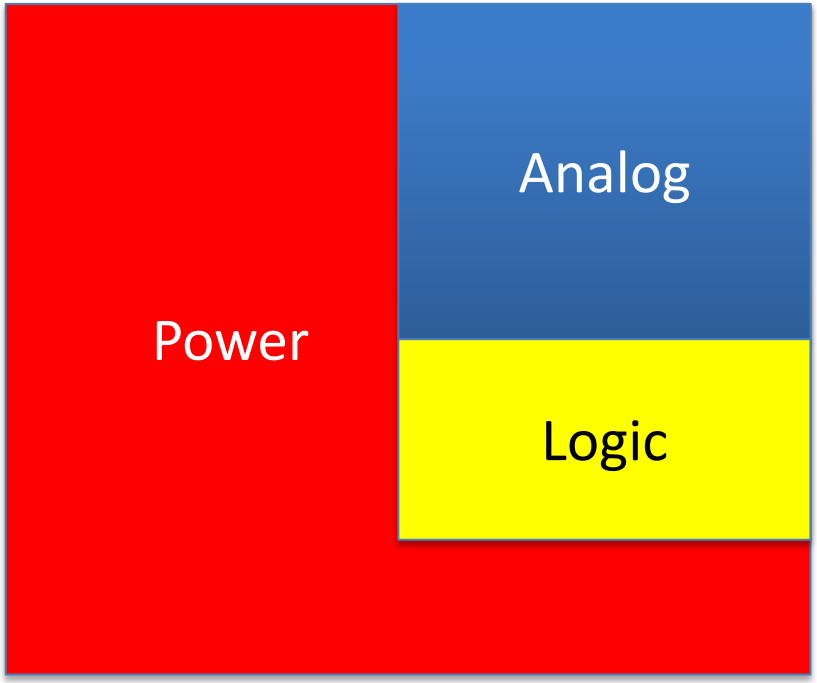
# MST™ CMOS – Current Commercialisation Funnel


| Time Horizon | | Activities "In the Funnel" |
|---|---|---|
| **24 Months +** | Asian Logic IDM & US Fabless Company & Asian Foundry | Engineering Exchange under bilateral NDA |
| **18 – 21 Months** | US Logic IDM & US Analog IDM<br>Taiwanese Foundry<br>Asian Analog IDM<br>US Analog IDM | Project(s) and Timing under Negotiation<br>Partnership Proposals under Consideration |
| **6 – 18 Months** | Asian Analog -IDM<br>Memory IDM<br>Asian OEM * | Evaluation Agreement signed, Statement of Work in place, Evaluation work progressing |
| **O – 6 Months** | $$$ | Product Qualification using MST™ Technology<br>Initial Adoption – Mass Production |
| | $$$$$$ | Widespread MST™ Technology Penetration |

* Potential Joint Marketing Agreement

| IN THE FUNNEL ... | TIMING ... |
|---|---|
| **Three** Customers/Partners in the MST ™ Evaluation/Integration Phase | 6-18 Months to Goal |
| **Five** Customers/Partners in the Partnership Consideration Phase | 18-21 Months to Goal |
| **Three** Customers/Partners in Engineering Technical-Exchange Phase | 24 Months + to Goal |
| **One** OEM Working Partnership for customers Demos | In Progress - ongoing |

# CMOS MST™ - IC-Chip Size Impact on Mixed Signal Product




**Expected MST™ Benefits:**

- Mobility Improvement for electrons and holes (P &N-Channel)
- Matching improvement due to low variability

**Impact on Chip Area:**

| | |
|---|---|
| Power Section Area savings – driven by mobility | 10% |
| Analog Section Area Saving – driven by Matching | 1.1% |
| Analog Section Area Saving – driven by Mobility | 2.5% |
| Logic Section Area Savings – driven by Mobility | 1.0% |
| **Total Area Savings = Chip Size Reduction:** | **14.3%** |

**30 V BCD Product Lay-out:**

Typical PMIC with chip are break-out

- Power 60%
- Analog 25%
- Logic 15%

Definitions:
BCD: BiCMOS Device (CMOS & Bipolar)
PMIC: Power Management IC
**Source:** LH Consulting, Dallas, TX

**Economic Impact:**

| | |
|---|---|
| Wafer Cost for 180nm BCD Process (200mm wafer) | $625 |
| Cost Savings for 14% Die Size Reduction (more chips/wafer) | $90 |
| Process Cost Adder for MST™ Film (incl. Mears Royalty) | $50 |

**Customer Process Cost Savings (more chips per wafer out) = $40 or 6.4%**

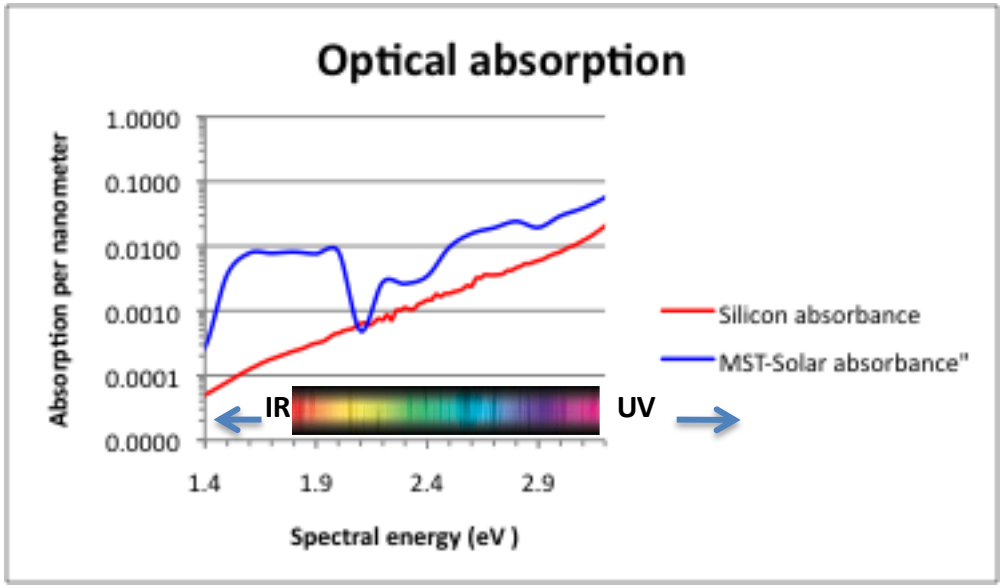
**Customer/Mears Win-Win:**

- Typical 200mm wafer fab runs 30k wafers/month; assuming 20% MST™ conversion equals annual savings of almost $3 mil.
- Mears Royalty Revenue ($15/wafer) at same time is about $1 mil/a

# MEARS Solar

**Overview:**

- MST-Solar has been demonstrated by experimental optical characterization* of fabricated MST-solar wafers to have significantly greater optical absorption per unit thickness compared to regular silicon.
- Optical results supported by fundamental physics simulation of MST-Solar film.
- Funding agreement between MEARS and K2 Energy Ltd established in 2010.




** Optical ellipsometry at Harvard Center for Nanoscale Systems, verified at UC Berkeley Labs*

**Current Status:**

- Initial R&D phase completed using US R&D facility, now seeking joint development partner for further validation and development.
- In the process of engaging major solar/semiconductor company for evaluation and joint development under NDA.
- **Goal:** More efficient, thinner / lighter and potentially cheaper optical sensors and specialized PV cells

# Global Market Comps

| Company | Market Cap (USD) | 2012 Revenue & EBITDA (USD) | EV/EBITDA | Comments | Customers |
|---|---|---|---|---|---|
| **ARM Holdings plc (ARM.LSE)** **www.arm.com** | 12,316m | Revenue: 550m EBITDA: 211m | 56x | Design of microprocessors, physical IP, and related technology and software; and sale of development tools to enhance the performance of high-volume embedded applications. licenses and sells its technology and products to electronics companies, which in turn manufacture, market, and sell microprocessors, application-specific integrated circuits, and application-specific standard processors. | Most leading semiconductor companies |
| **Rambus, Inc. (RMBS.NAS)** **www.ranbus.com** | 598m | Revenue: 234m EBITDA: -3m | -169x | Founded in 1990 & listed in 1997. Designs, develops and licenses chip interface technologies & semiconductor memory architectures. Rambus is also developing world-changing products and services in security, advanced LED lighting and displays, and immersive mobile media | AMD, Fujitsu, Intel, NEC, Panasonic, Elpida, IBM, Sony, Toshiba |
| **Tessera Technologies, Inc. (TSRA.NAS)** **www.tessera.com** | 908m | Revenue: 234m EBITDA: 52m | 8.6x | Founded in 1990 & listed in 2003. Designs, develops and licenses miniturisation technologies and products for next-generation electronic devices. Micro-electronics solutions enable smaller, higher-functionality devices through chip-scale and wafer-level packaging, silicon-level interconnect and 3D packaging, as well as silent air cooling technology. | Intel, Texas Instruments, Toshiba, Micron and Infineon |
| **Soitec S.A. (SOH.PA)** **www.soitec.com** | 332m | Revenue: 290m EU EBITDA: -26m EU | -14.2x | World leader in generating and manufacturing revolutionary semiconductor materials for the electronics and energy industries. Technology to fabricate engineered wafers for the world's leading chipmakers, and holds exclusive rights to use and license this technology to third-party materials and process suppliers. | Global microelectronics leaders for consumer and mobile devices. |

Source: Capital IQ; Company Reports

# Capital Structure and Use of Funds

MEARS Technologies
Quantum Engineered Materials

K2 ENERGY LIMITED

## Pro Forma Capital Structure

| | |
|---|---|
| • Existing K2 Energy shares (m): | 244.0 |
| • Post 1-for-10 consolidation (m): | 24.4 (17%) |
| • Consideration shares to Mears (m): | 85.0 (60%) |
| • Placement shares[1] (m): | 33.3 (23%) |
| • Pro forma shares on issue (m): | 142.7 (100%) |
| • Market cap at $0.30/sh (A$m): | 42.8 |
| • Cash at Listing (A$m): | 11.0 |
| • Options[2,3] on issue at listing (m): | 7.43 |

## Use of Funds[1,4]

| | |
|---|---|
| • MST CMOS Commercialisation & Customer Engagement Activity | A$5.4m |
| • General Administration & Working Capital | A$3.9m |
| • Offer costs | A$0.7m |
| • **TOTAL FUNDS RAISED[1]** | **A$10.0m** |

## Pro-forma Register

| | |
|---|---|
| • Existing K2 Shareholders | 17% |
| • Mears Shareholders | 60% |
| • Placement Shares | 23% |
| • *Proposed Board & Management* | *~10%* |

1. *This assumes that the maximum subscription of A$10million is raised under the Offer and that no over subscriptions are accepted.*
2. *600,000 options will be exercisable at $2.00 each on or before 31/12/14; 4.8m options will be exercisable at $0.30 each on or before 28/2/18; 200,000 options will be exercisable at $0.30 each on or before that date that is 3years from the date of issue*
3. *Includes 5.4 million options to be issued to Mears Executives as part of the Acquisition.*
4. *Please note that this table is an estimate of the proposed Use of Funds and subject to change.*

# Indicative Transaction Timetable

| ACTIVITY | DATE |
|---|---|
| MEARS Shareholder Approval Received | 20 February 2013 |
| Investor Road Show | 25 February 2013 – 8 March 2013 |
| Placement Book Build & Allocation Letters | 11-13 March 2013 |
| Signed Firm Commitment Letters | 15 March 2013 |
| K2 Energy EGM (Shareholder Approval) & Suspension | 20 March 2013 |
| DvP Settlement of Placement | 22 March 2013 |
| Completion of MEARS Transaction and Allotment of Shares for the Acquisition and Placement | 25 March 2013 |
| Trading in Securities Reinstated by the ASX | 2 April 2013 |

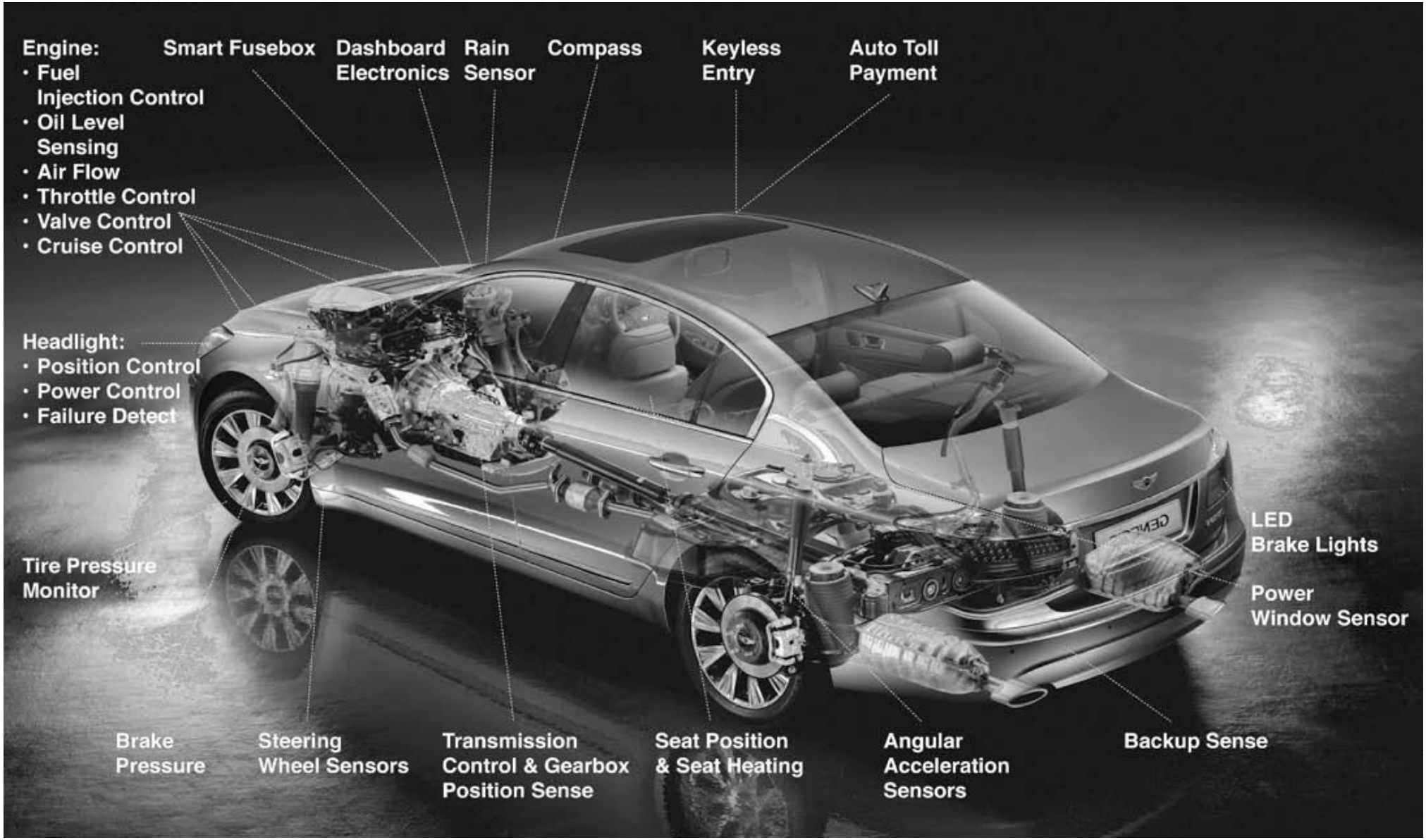
Note: All dates above may be subject to change.

# Contact Details

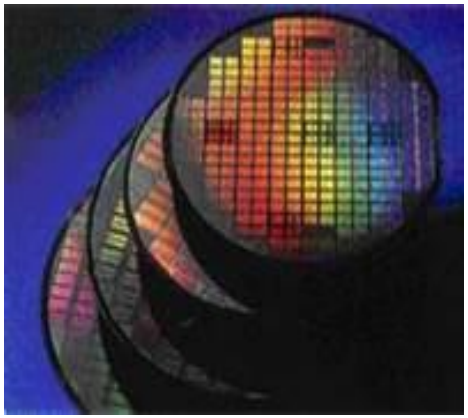
| MEARS Technologies Inc | K2 Energy Ltd | Foster Stockbroking |
|---|---|---|
| Erwin Trautmann (CEO)<br>+1 (214) 676-7349<br>erwin.trautmann@mearstechnologies.com<br><br>John Gerber (Chairman)<br>+1 (703) 801-4888<br>jdtgerber@gmail.com | Sam Gazal (Chairman)<br>+61 (2) 92513311<br>samgazal@ozemail.com.au | Stuart Foster<br>+61 (2) 99938131<br>stuart.foster@fostock.com.au<br><br>Martin Carolan<br>+61 (2) 99938168<br>martin.carolan@fostock.com.au |

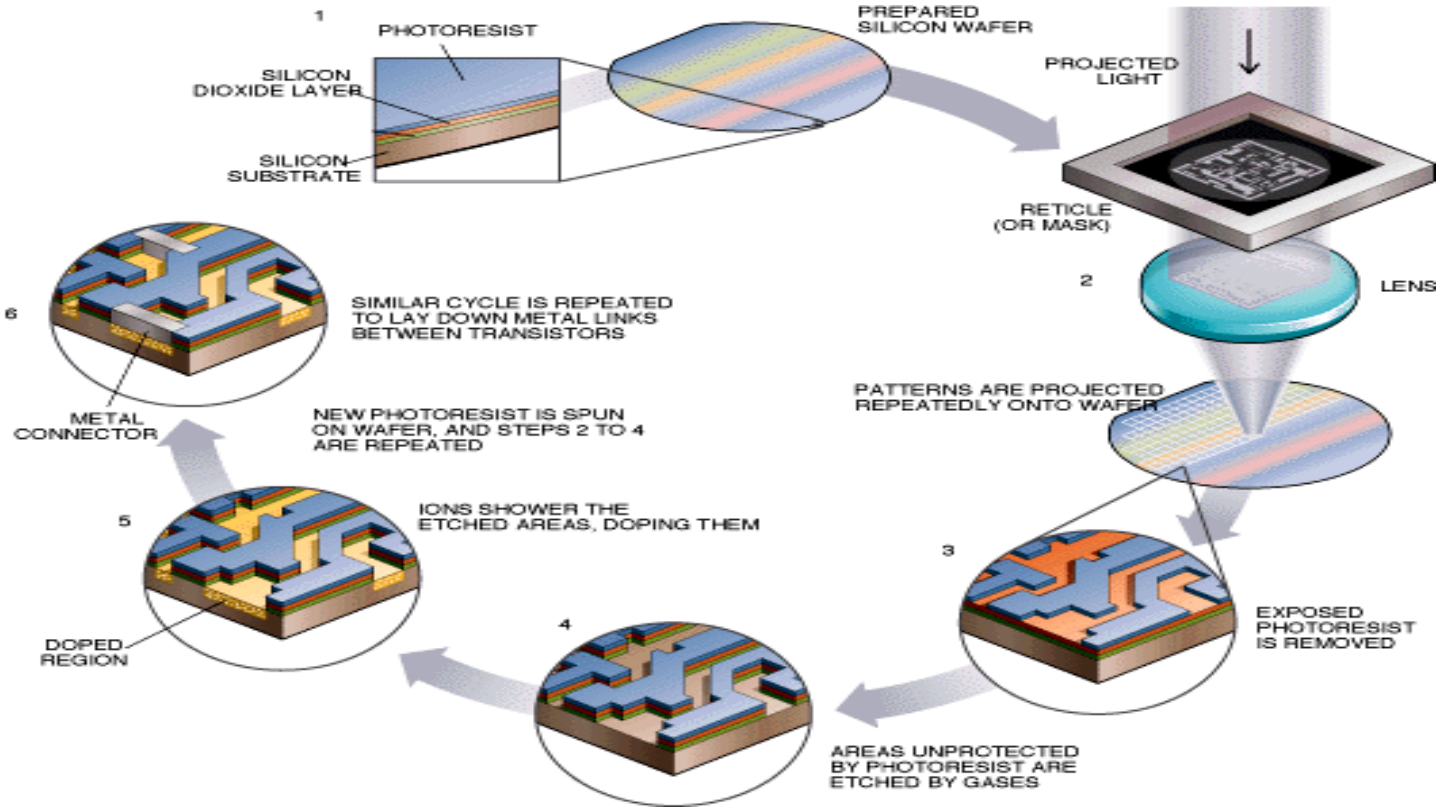
# Appendices

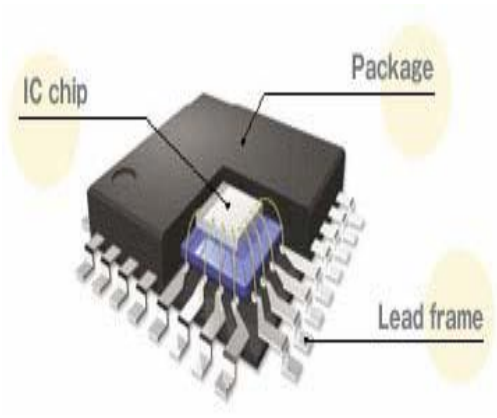
# Car Electronics Today

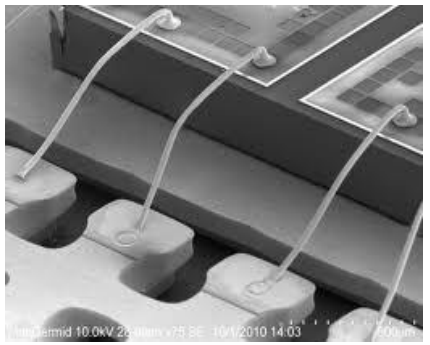


# IC Manufacturing – from Sand to Packaged IC





# IMPORTANT NOTICE AND DISCLAIMER

This investor presentation (Presentation) has been prepared by K2 Energy Limited (ABN 99 106 609 143) (K2) in relation to a placement of new ordinary shares in K2 (New Shares) under Section 708 of the Corporations Act 2001 (the Corporations Act).

**Summary Information**

This Presentation contains summary information about K2 and MEARS Technologies, Inc. (MEARS) as at the date of this Presentation. The information in this Presentation is of a general nature and does not purport to be complete nor does it contain all the information that an investor may require in evaluating a possible investment in K2 nor does it contain all the information which would be required in a disclosure document prepared in accordance with the requirements of the Corporations Act.

For further information relating to K2 see the periodic and continuous disclosure announcements lodged with Australian Securities Exchange (ASX) by K2 which are available on the ASX website. K2 will issue a notice under section 708A of the Corporations Act following completion of the placement of New Shares.

**Not a Disclosure Document**

This document is not a disclosure document under Australian law or under any other law. All offers made to a recipient of this Presentation (the Recipient )or any other person will be made without a disclosure document under Chapter 6D of the Corporations Act for example, by way of an invitation to a sophisticated investor or an invitation to a professional investor.

Accordingly, this document neither purports to be exhaustive nor contain all of the information which a prospective investor or the Recipient may require to make an investment decision and it does not contain all of the information which would otherwise be required by Australian law or any other law to be disclosed in a prospectus. The only representations or warranties in relation to the preparation of this document and the information in it (such as its accuracy, reliability or completeness) are those which are implied by law and which cannot be excluded by law. Otherwise, all such representations or warranties are excluded and the Recipient releases K2 and MEARS and their respective subsidiaries, officers, employees and advisers from any liability or responsibility for this document and indemnifies them against all such liability or responsibility brought by or through the Recipient or any successor in title.

**Future Performance**

All forward-looking statements in this document have been prepared by, or for K2 for internal use and have been included here for illustrative purposes only. They have been made on the basis of information available to K2 at the time of this document and are subject to uncertainties and contingencies, which are difficult to predict and many of which are beyond the control of K2 and its officers. Accordingly, all-forward looking statements must be read subject to these qualifications and no statement, warranty or representation is made that any forward looking statement will be achieved. K2 and MEARS and their respective officers, shareholders and advisors have no responsibility or obligation to inform Recipients of any matter arising or coming to their notice, after the date of this document, which may affect any matter referred to in this document.

**Past Performance**

Past performance information given in this document is given for illustrative purposes only and should not be relied on as (and is not) an indication of future performance.

# IMPORTANT NOTICE AND DISCLAIMER (cont.)

**Not Financial Advice**

This document does not contain financial advice and is not a recommendation to acquire shares in K2 and has been prepared without taking into account the objectives, financial situation or needs of individuals. Before making an investment decision prospective investors should consider the appropriateness of the information having regard to their own objectives, financial situation and needs and seek appropriate advice including financial, legal and taxation advice. K2is not licensed to provide financial product advice. Cooling off rights do not apply to the acquisition of securities in K2.

The document is provided to the Recipient on the basis that the Recipient must:

- make its own investigations and analyses regarding any information, statements or representations, opinions, estimates and projections contained in this document;
- satisfy itself to the extent it requires as to the conditions and prospects of K2 its business and affairs; and
- rely on their own inquiries and seek appropriate professional advice in relation to the information, statements or representations, opinions, estimates and projections in relation to K2 its business and affairs.

**Restriction on Distribution**

The distribution of this document in jurisdictions outside Australia may be restricted by law. Any Recipient who receives this document outside Australia must seek advice on and observe any such restrictions.

This document may not be released or distributed in the United States. This document does not constitute an offer to sell, or a solicitation of an offer to buy, securities in the United States.

Any securities described in this document have not been, and will not be, registered under the *Securities Act 1933* ("**US Securities Act**") and may not be offered or sold in the United States except in transactions exempt from, or not subject to, registration under the US Securities Act and applicable US State securities law.

**Investment Risk**

An investment in K2 shares is subject to investment and other known and unknown risks which are beyond the control of K2. K2 does not guarantee any particular rate of return or the performance of K2.

**Currency**

All amounts are presented in Australian dollars unless otherwise stated.